THE GENERAL RADIO Experimenter

VOLUME 43
NUMBERS 1, 2
JANUARY/FEBRUARY 1969

A DIGITAL FREQUENCY DIVIDER AND DELAY GENERATOR
NEW COUNTER FEATURES 35-MHz BANDWIDTH
1-GHz-BANDWIDTH AMPLIFIER DESIGN

The Cover: Prize-Winning Sculpture Uses GR Strobes

Experiments in Art and Technology (E.A.T.), a group involved in the interactions of artists and engineers, recently awarded a $1000 second prize to Mr. Frank Turner of Western Union for his engineering contribution to artist Wen-Ying Tsai's work "Cybernetic Sculpture."

The piece, which is based on the idea of harmonic motion, is made up of groups of nine-foot-high stainless-steel rods illuminated by stroboscopic light. Each rod is vibrated at its base, and the vibrations excite standing waves in the rods. When the surroundings are quiet, the strobes are synchronized with the mechanical-vibration frequency and the standing waves appear frozen. But sounds made by viewers frequency-modulate the flashing rate, causing the frozen standing waves to spring into shimmering, graceful undulations.

Mr. Tsai's work was recently on view at the New York Museum of Modern Art's exhibition, "The Machine as seen at the End of the Mechanical Age."

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The 1399 Digital Divider/Period and Delay Generator.

THE DIGITAL DIVIDER

A SYNTHESIZER FOR PERIOD AND DELAY

The 1399 Digital Divider/Period and Delay Generator bears the same relation to a conventional delay generator that a frequency synthesizer bears to a signal generator. With a frequency synthesizer we can obtain, for example, output frequencies up to 70 MHz in 10-Hz steps with the stability of the reference frequency. Analogously, the 1399 provides periods from 0.3 to 9,999,999.9 μs in increments of 0.1 μs when it is driven by its internal 10-MHz reference oscillator, and the accuracy and stability of the synthesized period are those of the reference.

Basically, the 1399 is a divider; it can divide any frequency from about 10 Hz up to more than 10 MHz by any selected integer from 3 to 99,999,999 – from a fractional frequency to a standard integral frequency, or vice versa. Since the instrument's circuitry is digital, practically the sole source of jitter is the derivation of the clock pulse from zero crossings of the reference signal. The output period consequently has remarkably little jitter; the stability of a 1-second output signal obtained by dividing a 1-volt, 10-MHz reference by 10^7 will typically be better than 10^{-12} second! The jitter in the output period would most likely be determined in this case by the second-to-second stability of the reference signal.

Simply throwing a front-panel switch converts the 1399 from a divider to a digital delay generator. While digital delay generators are now common laboratory tools, the unconventional circuitry of the 1399 makes it unique in this capacity: it is a digital delay generator *without recovery time*. It can, for example, produce 0.999,999,9-second delays at a 1.000,000,0-second rate! Ordinarily, the delay mode uses the precision internal time base, but, as in the divider mode, an arbitrary external signal can serve as the reference.

The 1399, like most recent GR instruments, has full external programming capabilities. All functions can be controlled remotely, most of them by low-current contact closures. The divider ratio or delay time, normally set on front-panel thumbwheel switches, can be externally controlled by switches, relays, or saturated NPN-transistor switches. The control-data format is either 1-2-4-8 or 1-2-4-2 BCD. To program a given decade externally, the corresponding thumbwheel is simply set to zero.

Figure 1. The 1399 and Loran C. An 1123 Syncronometer® digital time comparator, an 1124 Receiver, and two 1399's used to calibrate 1115-C Standard-Frequency Oscillators. The 1399's enable the system to derive time differences from a Loran system with arbitrary base rate.

APPLICATIONS

Delayed Sweep

It has been our experience that a device such as the 1399 is an essential oscilloscope accessory in examining time relationships in digital computers. Delay-sweep oscilloscopes ordinarily use analog delay systems, which exhibit excessive jitter when generating long delays. A coherent digital delay system does not suffer from this defect. The 1399, timed from the computer's clock, can be used to trigger a fast oscilloscope sweep. When the delay is initiated by one event, a subsequent event can be displayed on the oscilloscope screen with minimum jitter.

Counter-Readout Testing

The 1399 has proved to be the economical solution to a problem in our own calibration laboratory. In the final checkout of our counters, we switch on every digit sequentially in every decade of the readout in order to check the data-output wiring and the gas readout tubes. To do this, the 1399 is programmed to generate successive intervals of 1,111,111.1 μs, 2,222,222.2 μs, etc. While a frequency synthesizer could do the same job, the 1399 ties down a smaller investment in instrumentation.

Counter Accessory

As an accessory to a counter, the 1399 can be used to scale down the standard frequency by a ratio chosen at will in order to provide an arbitrary interval for the count. Or the 1399 can be used to count events and to gate the counter, which then measures elapsed time.

Digital Frequency Synthesizer

The development of the dividing scheme that has been used in the 1399 was undertaken originally in connection with a project to design a digital frequency synthesizer. Special-purpose synthesizers based on digital division are now quite common. Their strong point is the small number of tuned circuits required; thus, they are compact and require almost no setup adjustment.

A frequency-synthesizer scheme based on digital division is shown in Figure 2. The oscillator can be phase-locked to harmonics of the standard frequency f_s. If f_s were one hertz, for example, the 1399 would lock the oscillator at every hertz from about 10 Hz to over 10 MHz. Coarse tuning of the oscillator can be done manually, or it can be done automatically by adding a discriminator at the scale-of-N output.

The disadvantage of the digital-divider synthesizer of Figure 2 is the long settling time when the minimum frequency increment is small. Since the bandwidth of the filter in the phase detector's output has to be small compared with f_s, the phase-lock loop must have a time constant that is long compared with $\frac{1}{f_s}$ – perhaps 30 seconds if f_s were 1 Hz.

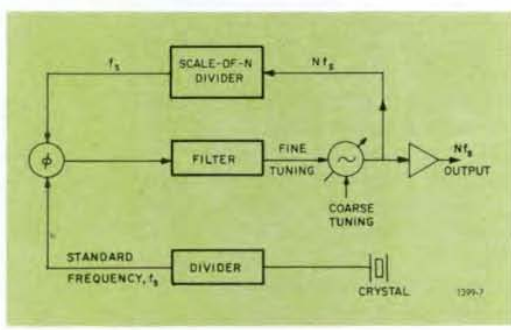


Figure 2. A digital-divider frequency synthesizer.

SPECIFICATIONS

Frequency Divider Ratio: 3:1 to 99,999,999:1. Delay range, 3 to 99,999,999 clock time-intervals, i.e., 0.3 μs to 9,999,999,9 s with 10-MHz clock.

Delay Accuracy: Delay interval varies from 0 to 1 clock interval when clock and start signals are not coherent.

INPUT CHARACTERISTICS Clock and delay-start inputs are identical except for max frequency (rate).

Rate: Delay-start input, 100 Hz to 2.5 MHz. Ext clock input, max > 10 MHz, typically 12 MHz; min, 100 Hz for 1-V pk-pk sensitivity, lower frequency with reduced sensitivity.

Sensitivity: 100 mV rms; will accept waveform of arbitrary shape.

Input Impedance: Approx 100 kΩ‖30 pF.

Trigger Threshold: ±1 V dc offset.

Trigger Polarity: Positive or negative, switch-selected.

INTERNAL CLOCK OSCILLATOR

Frequency Control: 10-MHz third-overtone quartz crystal in proportional-control oven.

Temperature: < 1 ppm, 0°C to 50°C.

Warmup: Within 1 ppm from room temperature in 10 min.

Short-Term Stability: 1×10^{-7} for 1-s sampling interval.

Long-Term Stability: 1×10^{-6} per year; with oscillator running continuously, $< 3 \times 10^{-9}$ per day after one month of operation.

Internal Clock Output: 1 V rms into 50 Ω.

Output Pulse: 5 V behind 50 Ω positive and negative available simultaneously. Duration approx 15 ns

PROGRAMMABILITY All functions and control settings, except trigger threshold, controlled by single contact closures to chassis ground. Max current, 2 mA through closed contact; max voltage drop, 150 mV across closed contact.

Divider/Delay Control: 1-2-4-8 BCD; DTL logic levels or contact closures.

Trigger Threshold: 0 to +10 V into approx 100 kΩ produces −1 to +1-V threshold detection.

Power Required: 100 to 125 or 200 to 250 V switch selected, 50 to 400 Hz, 20 W.

Accessories Supplied: Power cord, spare fuses, and mounting hardware with the rack model.

Mounting: Bench model (in metal cabinet) or rack model.

Dimensions (width X height X depth): Bench, 19 1/2 X 4 7/8 X 17 in. (495 X 125 X 435 mm); rack, 19 X 3 1/2 X 16 in. (485 X 89 X 410 mm).

Net Weight: Bench, 28 lb (13 kg); rack, 21 lb (10 kg).

Shipping Weight (est): Bench, 43 lb (20 kg); rack, 36 lb (16.5 kg).

Catalog Number	Description
	1399 Digital Divider/Period and Delay Generator
1399-9801	Bench Model
1399-9811	Rack Model

HOW IT WORKS: GET READY; GET SET; GO!

A functional diagram of the 1399 is shown in Figure 3. A 10-MHz third-overtone crystal in a proportional oven produces the 0.1-μs internal clock signal. The clock can also be an external signal of a few hertz to over 10 MHz. A gate determines whether the divider will run continuously, for the divide mode, or start on command of an external signal, for the delay mode. Both the delay-start and external-clock inputs have slope and threshold controls for establishing the trigger pulses from well-defined portions of the input signals. These input-trigger circuits are similar to those in most counters. The 1399's output circuit produces brief (15-ns), high-energy (±5 V behind 50 ohms) pulses that mark off the controlled interval.

The criteria for an arbitrary-scale divider were set down a number of years ago in a project at General Radio to develop a digital frequency synthesizer.[1,2,3] What was needed, simply, was a system that would produce one output pulse for every *N*th input pulse. It was hoped that the more significant decades could be slower, as they are in a counter – an important design objective, because fast flip-flops were, and still are, more expensive, more power hungry, and less reliable than slower ones. Ideally, the maximum counting rate of the scale-of-*N* should not be much less than the resolution of the first flip-flop in the fastest-counting decade. These were the goals. As the design of an actual circuit proceeded, there became apparent two rather fundamental obstacles to the use of conventional counting schemes in a frequency divider.

[1] R. W. Stuart, "A High Speed Digital Frequency Divider of Arbitrary Scale," *1954 IRE Convention Record*, Part 10.

[2] R. W. Frank, "A Computer Type Decade Frequency Synthesizer," *1954 IRE Convention Record*, Part 10.

[3] Work done under Contract DA 36-039 SC-15542, Signal Corps Engineering Laboratories, Ft. Monmouth, New Jersey.

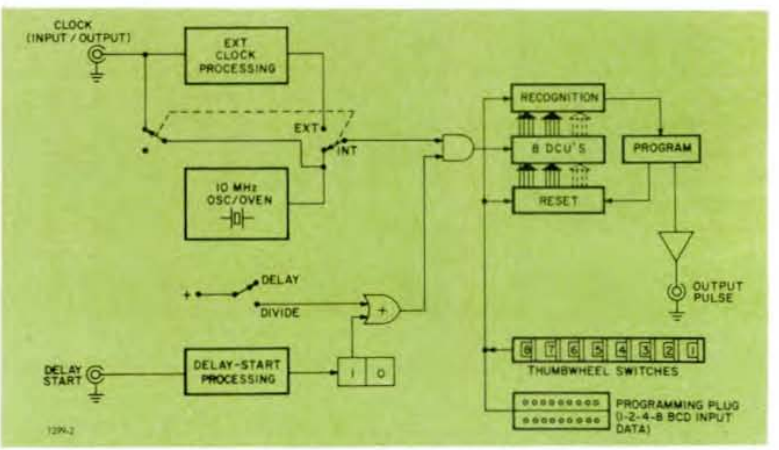


Figure 3. Functional diagram of the Type 1399 Digital Divider/Period and Delay Generator.

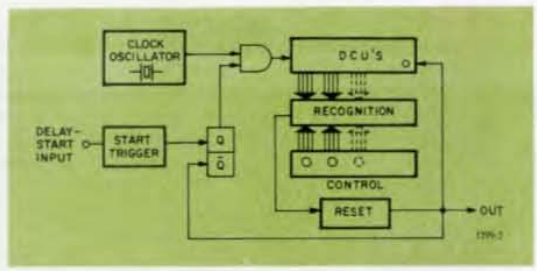


Figure 4. Simple delay generator based on digit recognition.

Figure 4 shows a simple delay generator based on digit recognition. At the first clock pulse after the gate is opened, the decade counting units (DCU's) begin to accumulate. They fill to the recognition state established by the controls, whereupon an output pulse is generated and the DCU's are reset to zero. If the duty ratio of the delay is not very high, the reset interval can last long enough to reset the slowest decade.

The problem with this simple delay scheme is the time required for propagation through the registers. If, by the time the last decade has reached its recognition state, the first one has moved on, recognition will not occur. This limit is reached rather quickly; five consecutive flip-flops, each with a delay of 20% of its resolution (a typical value), will cause a recognition failure at the maximum clock frequency even if all flip-flops are equally fast (which would be a violation of the first of our design criteria).

Figure 5 shows a scale-of-N divider. It is similar to the delay circuit just discussed, but it must divide continuously. This requirement compounds our problems: not only do we have to achieve reliable recognition, we must also complete the reset in less than one clock period. The situation has one hopeful circumstance, however. *If there is time to reset the highest-speed decade, then there is plenty of time to reset the others before they start to accumulate counts (10 clock periods for the second decade, 100 for the third, etc).*

There is another well-known way to achieve scale-of-N division when clock rates are not too fast. Figure 6 shows a circuit that recognizes only one state, namely, the output carry of the last decade. The division integer is determined by the *reset* state of the DCU's: the decades are reset to the complement of the desired divisor. Here there is no worry about time delays interfering with recognition; but we have traded that problem for another: there is not enough time for resetting. Suppose our divisor ends in the digits 001. The corresponding three DCU's would have to be preset to the complement 999. The first clock pulse after reset would carry straight through these three digits, changing them to zeros, and spill over into the fourth. The trouble is that this would have to happen before the slower second, third, and fourth DCU's had had time to reset. There is not even one full clock period available for resetting, because the reset pulse cannot occur until the output-initiating clock pulse (which changes *all* the digits from nines to zeros) has propagated through the entire counting register.

By now it will be clear that each of the two basic scale-of-N dividing schemes is plagued by a different problem. The reset-one-state-and-recognize-ten-states system suffers from recognition failure due to cumulative time delay, while the reset-ten-states-and-recognize-one-state system suffers from inadequate resetting time. One might wonder if a combination of the two methods could yield a workable system – and in fact it does.

Each DCU must have ten distinct states. We have talked about systems in which the DCU's have ten recognition states and one reset state, and systems in which they have one recognition state and ten reset states. Table 1 shows an intermediate scheme of 2 reset and 5 recognition states. In this system, a decade has to accumulate at least five counts following a carry before it is in a recognition state. Therefore every decade after the first remains in a recognition state for at least 5 preceding-decade pulses, waiting for the preceding decade to reach recognition. Furthermore, since decades are reset to no more than 5, every decade after the first will have five preceding-decade pulses in which to be reset. The reader might like to work out for himself the details of the reset-5-recognize-2 system shown in Table 2. It turns out to be only a little less efficient than the reset-2-recognize-5 system just discussed.

These examples of counting systems with mixtures of reset and recognition states demonstrate that an appropriate choice of coding can solve the recognition and reset problems that are inherent in the basic divider arrangements. We have seen that, with either of the two codings just described, first, the slower DCU's are waiting at their recognition states for the faster ones to catch up, and, second, all the DCU's (except the first) have plenty of time to reset before they have to begin counting.

The remaining limitation on the counting speed is the delay associated with carries between flip-flops in the first decade. Actual delays between

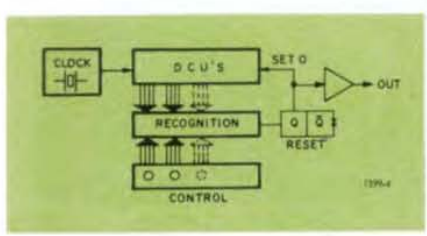


Figure 5. Simple scale-of-N divider. Like the delay generator of Figure 4, this circuit depends on digit recognition.

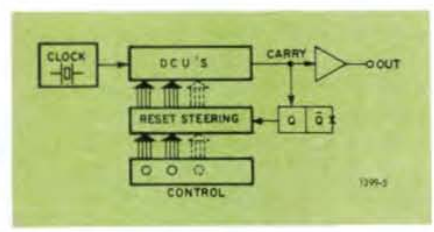


Figure 6. An alternative scale-of-N divider. This circuit recognizes only one state: all DCU's at zero. The count starts with the DCU's preset to the complement of the divisor.

Table 1
Reset-2-recognize-5 system

number	reset	recognize
0	5	5
1	5	6
2	5	7
3	5	8
4	5	9
5	0	5
6	0	6
7	0	7
8	0	8
9	0	9

Table 2
Reset-5-recognize-2 system

number	reset	recognize
0	4	4
1	3	4
2	2	4
3	1	4
4	0	4
5	4	9
6	3	9
7	2	9
8	1	9
9	0	9

Table 3
Reset-4-recognize-3 system. This is essentially the coding used in the 1399.

number	reset	recognize
0	5	5
1	4	5
2	5	7
3	4	7
4	1	5
5	0	5
6	1	7
7	0	7
8	1	9
9	0	9

the various digits will depend on the logical design of the DCU, but the source of delay is always the same: it is the carry generated by the 1-to-0 transition of an individual flip-flop. Now, since *odd* digits are counted by a 0-to-1 transition of only the *first* flip-flop, there is no delay problem with the odd digits. With our reset-2-recognize-5 coding, for example, serious delays occur at the numbers 6 and 8. If we could find a reset-recognition scheme in which only odd numbers have to be recognized, we would have attained our goal of a system whose counting speed is limited only by the resolution of the first flip-flop.

Table 3 shows a reset-4-recognize-3 coding scheme that is essentially similar to the one adopted for the 1399. Like the 2-5 and 5-2 systems, this system resets to no number greater than 5 and recognizes no number less than 5, so that it, too, overcomes the reset-time and propagation-delay difficulties. In addition, this system requires the recognition of only odd numbers.

Let us see how a system with 4-3 coding deals with the awkward divisor 00 000 003. The seven more significant DCU's will be reset to their recognition states of 5, and the first DCU will be reset to 4 (0010). The clock will now advance the first DCU to 7 (1110), and the 6-to-7 (0110-to-1110) transition will establish recognition and reset the first DCU to 4. Since recognition and reset involve transitions of the first flip-flop from 0 to 1 and back to 0 all within one clock period, the system will run half as fast as the first flip-flop – if there are no reset delays. In practice, reset delays would cause a further slight reduction in the speed of the system.

A modification[4] of the 4-3 system permits the 1399 to count at very nearly the speed of the first flip-flop. The trick is to delay the start of the count by two clock periods to allow enough time for the first flip-flop to reset. Refer to the 1399's programming diagram, shown in Figure 7. While counting is in progress, *FF1* is in its Q state, the clock gate is open, and the output gate is closed. Recognition operates *FF1* to Q, thus closing the clock gate, opening the output gate, and triggering the reset-pulse generator. The first clock pulse following recognition passes through the output gate and switches *FF2* to Q. The next clock pulse switches *FF2* back to $\bar{Q}$, thereby triggering the output pulse, resetting *FF1* to Q, closing the output gate, opening the clock gate, and beginning the next count. Counting has been interrupted for two clock periods, allowing plenty of time to reset the first decade. The two missed counts are compensated for by making the first decade recognize 3's, 5's, and 7's instead of 5's, 7's, and 9's. The small price we have to pay for the additional speed is that the system is unable to divide by two, a trivial operation that can be done by one flip-flop. (As a matter of fact, two clock periods are more than enough time for resetting, but skipping just one pulse would require that even numbers be recognized in the first decade.)

—R. W. Frank

A brief biography of Mr. Frank appeared in the November-December, 1967 issue of the *Experimenter*.

[4] U.S. Patent No. 3,050,685.

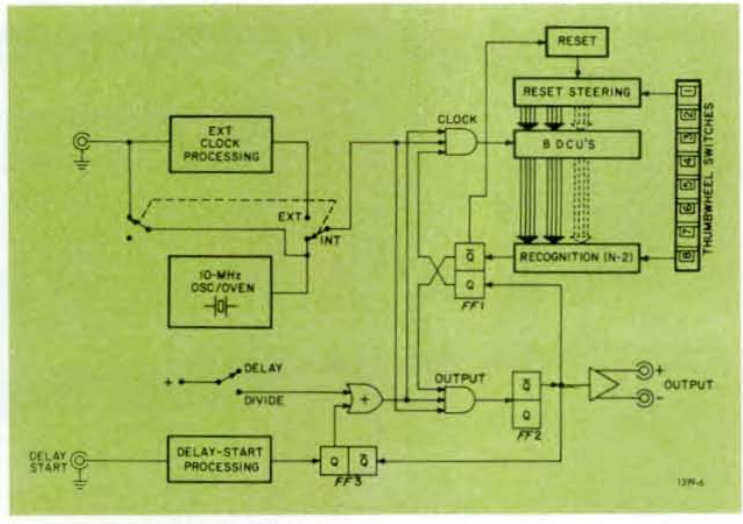


Figure 7. Internal programming of the 1399.

The new 1191-B Counter.

1191 COUNTER NOW FEATURES 35–MHz BANDWIDTH

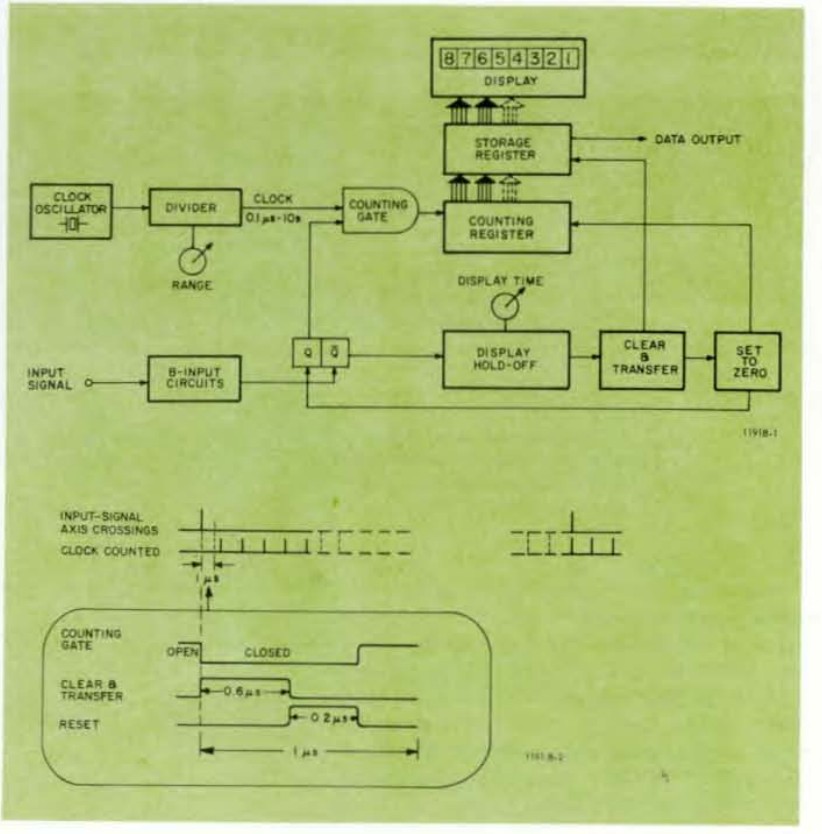
• "Strobed" single-period measurement • 1-μs data holdoff • Improved time-interval mode • Crystal-oven standby power

The 1191 is an integrated-circuit counter/timer for measuring frequency, period, average period, frequency ratio, and time interval. (See the November-December 1967, *Experimenter* for a complete description.)

The new 1191-B offers several significant improvements over its predecessor, and at the same base price. Foremost among these are the increased frequency range – the upper limit is now 35 MHz – and a unique "strobed" single-period mode, in which the 1191-B makes period measurements with virtually a 100-percent duty cycle.

Like its predecessor, the 1191-B is available in combination with either of two GR scalers as the 1191-Z. The combination offers all the features of the counter alone, plus operation up to 500 MHz. The bench version of the 1191-Z has the counter and scaler in a single cabinet.

The 1191-Z Counter. The 500-MHz model is shown here in its bench version.



Program of "strobed" period measurement.

"Strobed" Period Measurement

Many measurements require that the counter extract information from the input signal at the maximum possible rate. Ordinarily, a counter measurement of the period of a signal is inefficient from an information-gathering point of view. The period mode is conventionally programmed so that a pair of consecutive signal axis crossings open and close the counting gate. The closing of the gate initiates a hold-off period (often as long as 0.1 second) during which the data is transferred to storage. At the end of the hold-off period the counter is ready to make a new measurement. The duty ratio of such a program can be no more than 50 percent, and it can be this high only if the hold-off period can be made brief enough to allow counting during alternate cycles.

The unique "strobed" period mode of the 1191-B permits the new counter to gather data during almost 100 percent of the time. The internal program of this measurement is shown in the accompanying block and timing diagrams. *Every* input-signal axis crossing initiates an operation in which the accumulated count is transferred to storage, the counting register is reset to zero, and a new count is begun.

Catalog Number	Description
	1191-B Counter
1191-9710	Bench Model
1191-9711	Rack Model
1191-9712	Bench Model with Data-Ouput Option
1191-9713	Rack Model with Data-Output Option
1191-9714	Bench Model with High-Precision Time-Base Option
1191-9715	Rack Model with High-Precision Time-Base Option
1191-9716	Bench Model with both Options
1191-9717	Rack Model with both Options
	1191-Z Counter (100 MHz)
1191-9900	Bench Model with both Options
1191-9901	Rack Model with both Options
	1191-Z Counter (500 MHz)
1191-9902	Bench Model with both Options
1191-9903	Rack Model with both Options
1158-9600	**P6006 Probe**, Tektronix Catalog No. 010-0127-00 (not sold separately)

If the last-counted clock pulse in a given measured period has to propagate through all eight decades of the counting register, approximately 0.6 μs will elapse after the counting gate closes before the counting register has settled and the data are in storage. Another 0.2 μs is needed to reset the counting register to zero. Thus, with the DISPLAY TIME set to its minimum position (1 μs), the total dead time – the time at the beginning of a measured period before the counting gate opens – is about 0.8 μs. Except at the fastest clock rate (0.1 μs), only a single clock pulse may not get counted because of the dead time, and the probability of missing a pulse decreases by an order of magnitude as the clock rate decreases by an order of magnitude. One can easily determine the precise amount of dead time by measuring an accurately known period with the internal clock set at 0.1 μs. The discrepancy between the count and the known period will be between 0.7 and 0.9 μs.

Wideband Amplifier Design

by M. Khazam

This article derives the formulas (in terms of y-parameters) for constructing transistor constant-gain circles on a load-admittance Smith chart. An input-admittance grid constructed on the same chart provides a direct readout of the input admittance. A design example using transmission lines as matching elements is given.

Amplifiers with bandwidths in excess of 1 GHz have become quite practicable with the introduction of high-frequency transistors. Feedback equalization of gain over such wide bandwidths is difficult, partly because of the complex feedback networks that would have to be used and partly because there is often insufficient open-loop gain. In this article we outline a procedure for designing the type of wideband amplifier that is incorporated in the Type 1237 VHF/UHF Preamplifier.

Two-port Power Gain

The y-parameters of a two-port network are defined by the well-known relations

$$\left.\begin{aligned} I_1 &= y_{11} V_1 + y_{12} V_2 \\ I_2 &= y_{21} V_1 + y_{22} V_2 \end{aligned}\right\} \quad (1)$$

Figure 1

where the signs of voltages and currents are those of Figure 1. If Y_L is the load admittance and Y_S the source admittance, then the input and output admittances are given by

$$Y_{in} = y_{11} - \frac{y_{12}\, y_{21}}{y_{22} + Y_L} \quad (2)$$

$$Y_{out} = y_{22} - \frac{y_{12}\, y_{21}}{y_{11} + Y_S} \quad (3)$$

The power flowing from the source into the network is

$$P_{in} = |V_1|^2 \ \mathcal{R}e\, Y_{in}$$

and the power flowing out of the network into the load is

$$P_{out} = |V_1|^2 \left|\frac{y_{21}}{y_{22} + Y_L}\right|^2 \mathcal{R}e\, Y_L$$

The power-gain ratio is thus

$$\mathcal{G} = \frac{P_{out}}{P_{in}} = \frac{\mathcal{R}e\, Y_L}{\mathcal{R}e\, Y_{in}} \left|\frac{y_{21}}{y_{22} + Y_L}\right|^2 \quad (4)$$

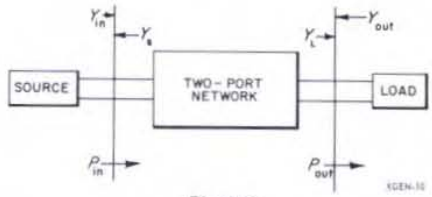


Figure 2

The more significant transducer gain $\mathcal{G}_T$, defined as (power to load) ÷ (source's available power), is related to the power gain $\mathcal{G}$ by

$$\mathcal{G}_T\,(\text{dB}) = \mathcal{G}(\text{dB}) - \text{input mismatch loss (dB)} \quad (5)$$

Gain Circles On the Load-Admittance Smith Chart

We define a normalized load admittance y by

$$y = g + jb \equiv \frac{\mathcal{R}e\, Y_L}{\mathcal{R}e\, y_{22}} + j\,\frac{\mathcal{I}m\, Y_L + \mathcal{I}m\, y_{22}}{\mathcal{R}e\, y_{22}} \quad (6)$$

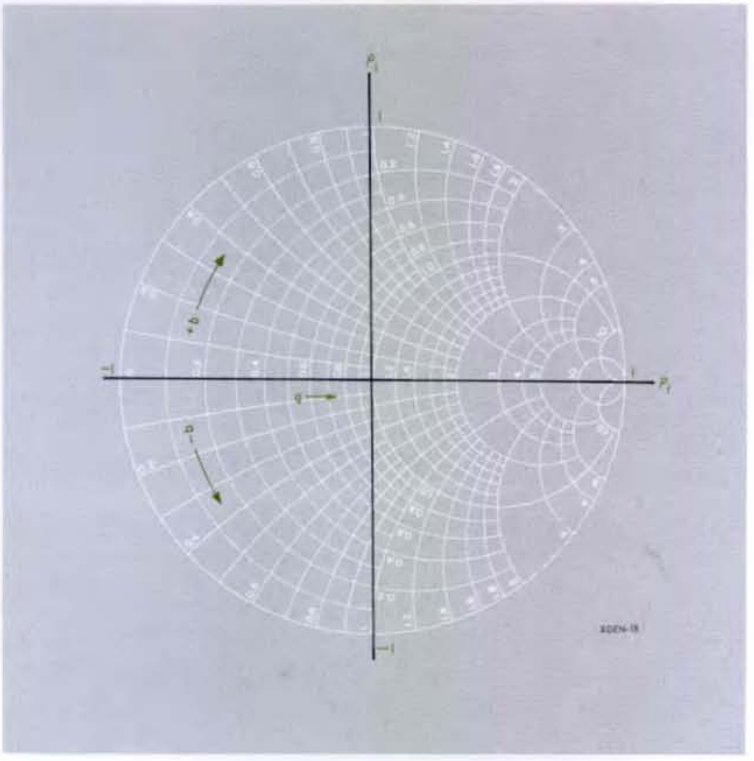


Figure 3. The relation between y and ρ.

Note that the imaginary part of y includes $\mathcal{B}_m y_{22}$ along with $\mathcal{B}_m Y_L$. Since g and b may vary over wide ranges of values, we would find ourselves constructing rather unwieldy charts if we continued to work directly with y. Accordingly we make a transformation to a new variable ρ:

$$\rho = \frac{y - 1}{y + 1} \tag{7}$$

(Note that ρ is the negative of the reflection coefficient, as conventionally defined.) If we write ρ_r and ρ_i for the real and imaginary parts of ρ, the expression (4) for the power-gain ratio can be recast in the following form:

$$\left(\rho_r + \frac{g_t \mathcal{G}}{|y_{21}|^2}\right)^2 + \left(\rho_i - \frac{b_t \mathcal{G}}{|y_{21}|^2}\right)^2 = r^2 \tag{8}$$

where

$$r = \sqrt{1 - 2\mathcal{G}\,\frac{2g_{11}g_{22} - g_t}{|y_{21}|^2} + \mathcal{G}^2\,\frac{|y_{12}|^2}{|y_{21}|^2}} \tag{9}$$

We have used the notation $y_{11} = g_{11} + jb_{11}$, $y_{22} = g_{22} + jb_{22}$, and $y_{12}y_{21} = g_t + jb_t$.

Equation 8 represents a family of constant-gain circles on the ρ-plane. When $\mathcal{G} = 0$, the radius r is unity and the circle's center is at the origin of the ρ-plane (the circle coincides with the zero-conductance circle on the Smith chart). Provided the two-port is unconditionally stable, the radius decreases with increasing gain until a value of $\mathcal{G}$ is reached at which the radius is zero. The gain at this point, $\mathcal{G}_{max}$, is the maximum that can be achieved without external feedback, and the corresponding point on the ρ-plane represents a conjugate match between the two-port and the load. The centers of the circles,

$$\rho_r(\text{center}) = -\frac{g_t \mathcal{G}}{|y_{21}|^2}, \quad \rho_i(\text{center}) = \frac{b_t \mathcal{G}}{|y_{21}|^2}, \tag{10}$$

fall on the straight line through the origin of the ρ-plane that makes an angle

$$\phi = \tan^{-1}\left(-\frac{b_t}{g_t}\right) \tag{11}$$

with the positive ρ_r-axis. The distance from the centers to the origin of the ρ-plane is

$$d = \frac{|y_{12}|}{|y_{21}|}\,\mathcal{G} \tag{12}$$

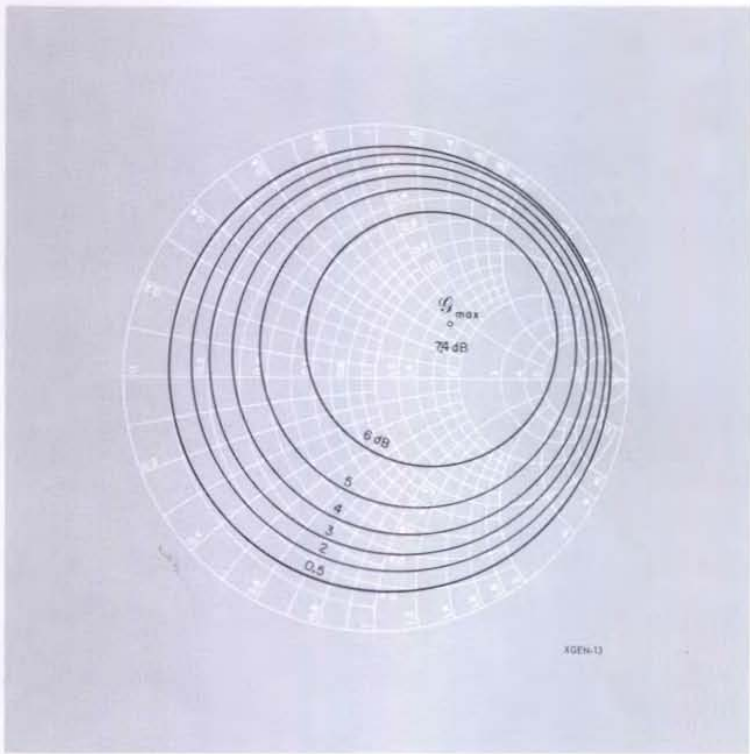


Figure 4. A set of constant-gain circles for a 2N3478 transistor at 900 MHz plotted on the load-admittance Smith chart.

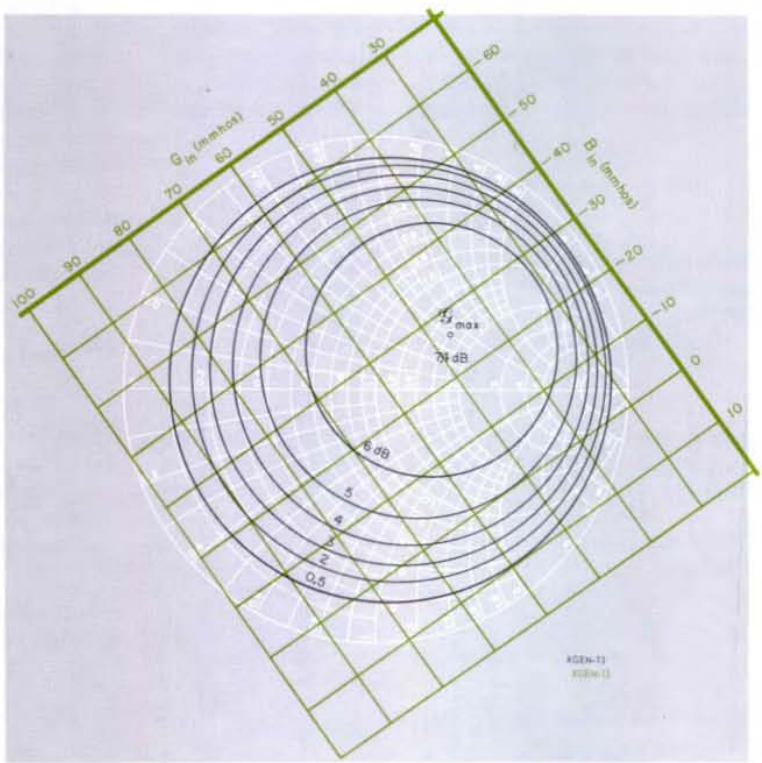


Figure 5. An input-admittance grid has been added to the chart of Figure 4.

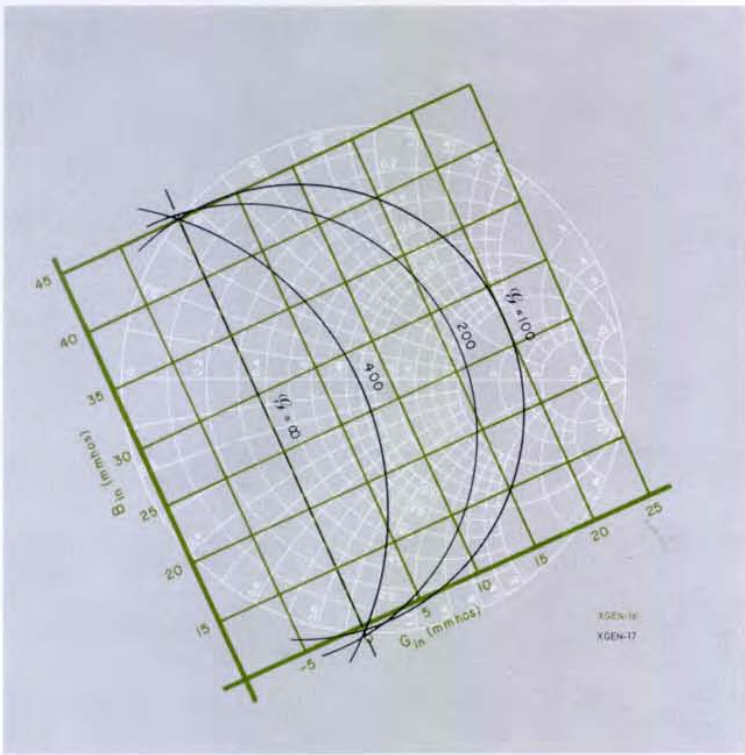


Figure 6. A potentially unstable situation. If the load admittance falls in the lower left of the chart beyond $\mathcal{G} = \infty$, the input conductance is negative and the two-port can oscillate.

Figure 4 shows a set of constant-gain circles for a 2N3478 transistor at 900 MHz, plotted on a Smith chart. The chart's normalized grid corresponds to our admittance variable y.

Input-Admittance Grid

To find the input admittance of the two-port, we return to equation 2:

$$Y_{in} \equiv G_{in} + jB_{in} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L} \tag{13}$$

If we replace Y_L on the right-hand side of (13) by the normalized load admittance y, defined by (6), and then make the transformation (7) to the ρ-plane, we get

$$\left.\begin{aligned} G_{in} &= \left(\frac{g_t}{2g_{22}}\right)\rho_r - \left(\frac{b_t}{2g_{22}}\right)\rho_i + \left(g_{11} - \frac{g_t}{2g_{22}}\right) \\ B_{in} &= \left(\frac{b_t}{2g_{22}}\right)\rho_r + \left(\frac{g_t}{2g_{22}}\right)\rho_i + \left(b_{11} - \frac{b_t}{2g_{22}}\right) \end{aligned}\right\} \tag{14}$$

These expressions represent a rectangular grid of G_{in} = constant and B_{in} = constant lines on the ρ-plane. We can construct this grid on our load-admittance chart if we will note the following relations between the G_{in}- and B_{in}-lines and the ρ_r- and ρ_i-axes. The spacing $\Delta\rho_r$ between the intercepts of consecutive G_{in} = constant lines with the ρ_r-axis is

$$\Delta\rho_r = \frac{2g_{22}}{g_t}\ \Delta G_{in} \tag{15}$$

where ΔG_{in} is the chosen increment in G_{in}. The spacing $\Delta\rho_i$ along the ρ_i-axis between B_{in}-line intercepts is given by the same relation (the G_{in}- and B_{in}-axes have the same scale factor):

$$\Delta\rho_i = \frac{2g_{22}}{g_t}\ \Delta B_{in} \tag{16}$$

The angle that the B_{in} = constant lines make with the ρ_r-axis is

$$\tan^{-1}\left(\frac{\Delta\rho_i}{\Delta\rho_r}\right)_{B_{in}\ =\ \text{const}} = \tan^{-1}\left(-\frac{b_t}{g_t}\right) \tag{17}$$

which is just the angle ϕ_t given by (11), of the line of centers of the constant-gain circles. The Y_{in}-grid has still to be positioned on the ρ-plane, and this requires the calculation of one point.

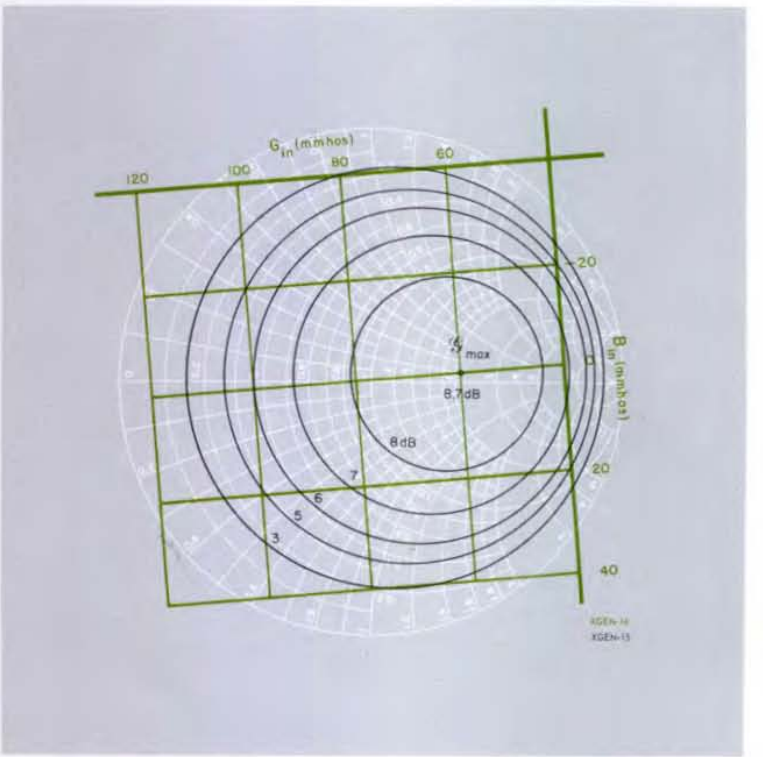


Figure 8. Design chart for the 2N3478 at 600 MHz.

Figure 5 shows an input-admittance grid superimposed on the gain-vs -load-admittance chart of Figure 4.

Stability

The constant-gain circles of Figures 4 and 5 are characteristic of a two-port that is unconditionally stable. An unconditionally stable two-port is one whose input admittance has a positive conductive component whenever the output admittance does, and vice versa.

A potentially unstable situation is illustrated in Figure 6, which shows a load-admittance-Smith-chart plot of the gain circles and input-admittance grid for a 2N3478 transistor plus feedback capacitor at 400 MHz. Notice that in this case the gain circles get larger with increasing gain and that there are negative values of G_{in} within the $g = 0$-circle, where the load conductance is positive. The $g = \infty$ "circle" coincides with the $G_{in} = 0$ line, and load admittances that fall to the right of this line will cause oscillation unless the source conductance is large enough that the total conductance at the input is not negative.

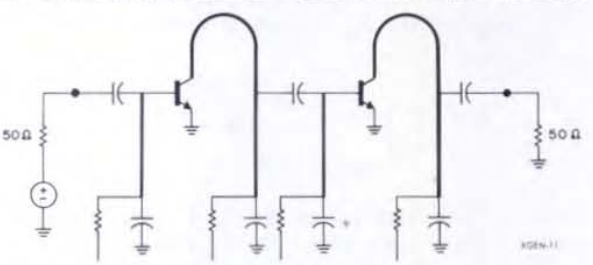


Figure 7. Two-stage wideband amplifier. Matching is accomplished by L-networks formed by series and shunt sections of line.

One can inspect the output admittance as a function of source admittance by constructing a rectangular output-admittance grid on the source- admittance Smith chart. The procedure is the same as that outlined for constructing the G_{in}– B_{in}–grid except that the subscript 1's and 2's on the y-parameters are interchanged.

A Design Example

Let us design a two-stage amplifier using 2N3478's. The analysis of a wideband amplifier by the method described in this article generally involves sampling the performance at a number of frequencies over the passband. Transistor parameters have to be measured and charts constructed at each frequency. For the sake of a simple example, though, let us set ourselves a fairly limited objective: more or less constant gain from 900 MHz down to 600 MHz or possibly lower. We will see what we can do with the circuit of Figure 7, in which the matching networks are simple series-and shunt-line L networks, and we will analyze the performance at only the two frequencies 900 and 600 MHz. We shall assume 50-ohm source and load impedances.

The design chart for 900 MHz is the one shown in Figure 5, and the chart for 600 MHz is shown in Figure 8. We find from the charts that the load admittance for maximum gain is 0.83 - j5.6 mmho at 900 MHz and 1.1 - j3.9 mmho at 600 MHz. Assuming that the matching networks will be etched on a circuit board, we select 125 ohms as a practical value for the characteristic impedance of the line sections.

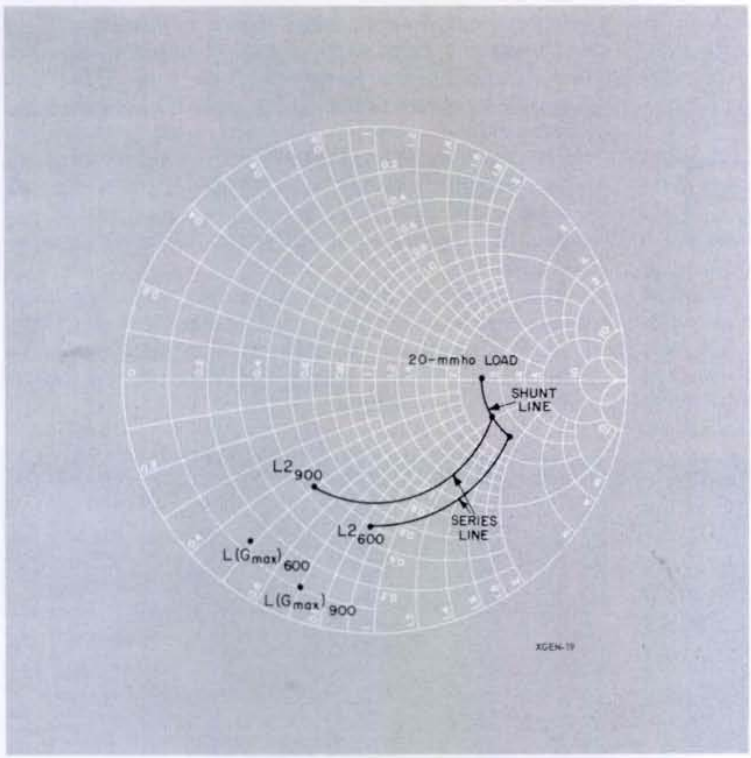


Figure 9. Transformation of the load admittance by the output network. The admittance grid is normalized to 8 mmhos (125 Ω).

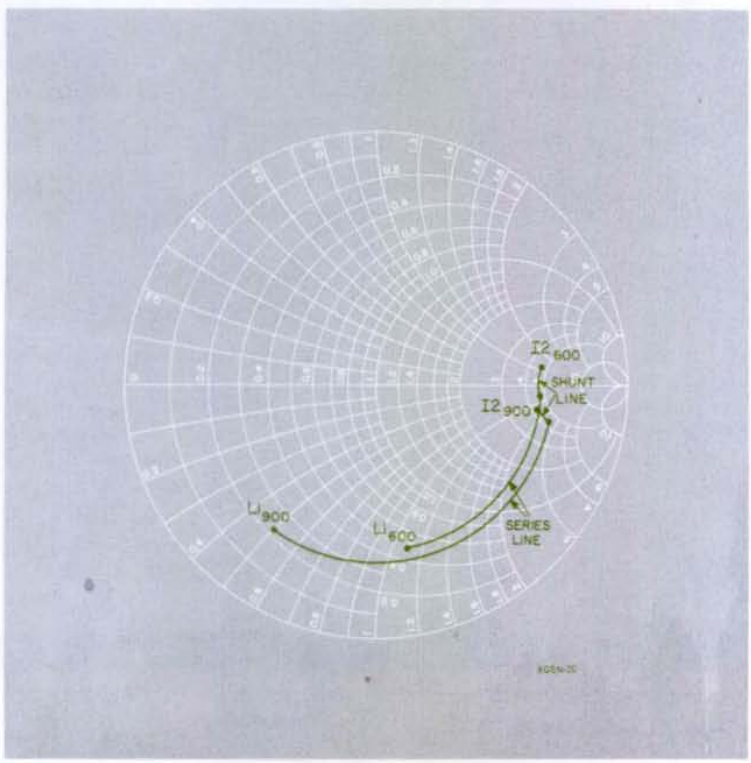


Figure 10. Admittance transformation by the interstage network.

Through a pencil-and-paper cut-and-try procedure, we arrive at an output network with a shunt-line length of 4.2 cm (electrical) and a series-line length of 4.7 cm. The admittance transformation performed by the output network is plotted on the Smith chart of Figure 9, which is normalized to 8 mmhos (125 ohms). The points $L2_{600}$ and $L2_{900}$ represent the loads that the network presents to the transistor at 600 and 900 MHz, and $L(\mathcal{G}_{max})_{600}$ and $L(\mathcal{G}_{max})_{900}$ are the load admittances for maximum gain at the two frequencies. When the admittances represented by $L2_{600}$ and $L2_{900}$ are renormalized to y_{22} and plotted on the charts of Figures 8 and 5, respectively, the gains that are found are 6 dB at 600 MHz and 5.1 dB at 900 MHz. Although we could probably do a better job of matching with higher-impedance line sections or with a more complicated network, we shall be content, for the purposes of our example, with these results.

We select an interstage network with shunt-line lengths that are again 4.2 cm and a series-line length of 5.25 cm. The transformation is plotted in Figure 10. The points $I2_{600}$ and $I2_{900}$ are the input admittances of the second stage, found from the G_{in}-B_{in}-grids of Figures 8 and 5 and normalized to 8 mmhos. The points $L1_{600}$ and $L1_{900}$ are the load admittances presented to the first transistor. When we renormalize $L1_{600}$ and $L1_{900}$ to y_{22} and plot them on Figures 8 and 5 respectively, we find gains of 4.9 dB at 600 MHz and 5.7 dB at 900 MHz for the first stage.

Figure 7 does not show a series-line section at the input of the amplifier. This is because we can do without an admittance-transforming series section at the input if we will tolerate a fairly small amount of mismatch loss. We find the admittances presented by the base of the first transistor by means of the G_{in}-B_{in}-grids of Figures 8 and 5. Adding the susceptance of the 4.2-cm input shunt line, we calculate that the mismatch-loss penalty for connecting the input directly to a 50-ohm source is 0.5 dB at 600 MHz and 0.7 dB at 900 MHz. If we accept these losses, the over-all gain of the amplifier is 10.4 dB at 600 MHz and 10.1 dB at 900 MHz.

This simplified example shows that, even with very simple matching networks, amplification over quite wide frequency ranges can be achieved with gains reasonably close to the optimum gain of the device at the highest frequency in the passband.

A brief biography of Mr. Khazam appeared in the July-August, 1967 issue of the *Experimenter*.

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